FIR Filter Design

Project 1 CE6325 VLSI Design: Verilog HDL

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Fall 2024

**Project Description:**

A Finite Impulse Response (FIR) filter was designed with pre-determined specifications. The filter order, and the Data\_in size were parameterized to allow the design to be scalable. The filter takes in a sample input, processes the sample input and passes it to an output register

**Design Specifications**

Filter order: 5

Filter coefficients: [7, 8, 9, 12, 4]

Data\_in size: 4

Data\_out size: 16

**Data flow of the design**

A diagram of a flowchart

Description automatically generated

Figure1: Finite Impulse Response (FIR) Filter using Multiply and Accumulate

**Design Netlist**

A diagram of a circuit

Description automatically generated

Figure 2: Netlist for the FIR filter

**Testbench Process Flow**

A diagram of a computer program

Description automatically generated

Figure 3: Shows the Testbench Process flow

Table 1 showing Filter out with when Data\_in = decimal (6)



Table 1 shows that Data\_in will go shift through all of Sample[k] when enough time is allowed before changing the value at the input. The value in each register of Sample[k] is multiplied by the filter coefficient (bn). The values of the multiply is accumulated or summed to form the output of the filter.

**Register Transfer Logic (RTL) Simulation Result**

Table3 shows the observed values from the simulation results

A screenshot of a computer

Description automatically generated

**Simulation Wave form**

A black screen with green lines and white text

Description automatically generated